JACKEY ZIJUN YAN

Electrical and Computer Engineering
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OBJECTIVE

To obtain an intern in the research area of Computer-Aided Design (CAD) on VLSI Physical Design.

EDUCATION

Ph.D.	Computer Engineering	Iowa State University (ISU), Ames, IA	Expected 2011
B.S.	Automation	Huazhong University of Sci.&Tech. (HUST), Wuhan, China	2006

RESEARCH INTERESTS

- VLSI Physical Design for Nanometer Scale Circuits
- Efficient Large-scale Floorplanning and Placement Algorithms
- Physical Synthesis Integrated System-on-Chip (SoC) Designs

ACADEMIC EXPERIENCE

Research Assistant VLSI CAD Lab., ISU March 2007 – Present

- Proposed the Generalized Slicing Tree, Enumerative Packing and Novel Block Swapping and Mirroring to be used in the multi-level fixed-outline floorplanning. A high-quality, fast, non-stochastic and scalable fixed-outline floorplanner *DeFer* was developed based on the above techniques.
- Currently working on the large-scale mixed-size placement algorithm.

Teaching Assistant Dept. of ECE, ISU August 2006 – March 2007

- Co-worked on a reverse engineering project on FPGA, from the bit-stream level to HDL level, and tried to find a new approach on energy saving and function optimization.
- Co-worked on a demonstrable FPGA platform against the practical real-world Side-Channel Attacks.
- Implemented the integration of *FastRoute* and *MOCSYN*. It is about the multi-core system synthesis with the physical interconnection awareness.

Research Assistant Renesas Embedded MCU Lab., HUST October 2004 – June 2006

- Developed a GPRS wireless communication system based on ARM and embedded Linux.
- Designed a mobile wireless sensor network for intelligent auto-motives, using Renesas M16C/62 micro-controllers.

Research Assistant ASIC Lab., HUST March 2004 – September 2004

- Designed the Multifunction Digital Clock System and Address Calculator.
- Programmed reconfigurable devices using Verilog HDL in MAX+plus II.

Research Assistant Institute of Automation, HUST March 2003 – February 2004

- Developed a CAD software, *Circuit Designer*, in MS-DOS environment using C language. It can draw simple circuit schematics with different electrical components by Graphical User Interface.

PROFESSIONAL EXPERIENCE

Intern Research Scientist Cadence Research Lab., Berkeley, CA May 2007 – August 2007

Supervisors: *Dr. Philip Chong and Dr. Christian Szegedy*

- Worked on the analog device placement with various geometry constraints, and co-developed a probability-based technique to solve this problem. This work involved the algorithm design, standardizing different constraints between industrial and academic interfaces, coding in C++ and Perl, and working with Cadence Virtuoso and Cadence OpenAccess.

PUBLICATIONS

Conference Papers

- **J. Z. Yan**, C. Chu and W. K. Mak, "SafeChoice: A Novel Clustering Algorithm for Wirelength-Driven Placement", to appear *in Proceedings of ACM International Symposium on Physical Design*, 2010.
- **J. Z. Yan**, N. Viswanathan and C. Chu, "Handling Complexities in Modern Large-Scale Mixed-Size Placement", *in Proceedings of IEEE/ACM Design Automation Conference*, pages 436-441, 2009.
- **J. Z. Yan** and C. Chu, "DeFer: Deferred Decision Making Enabled Fixed-Outline Floorplanner", *in Proceedings of IEEE/ACM Design Automation Conference*, pages 161-166, 2008. (**Nominated for DAC Best Paper Award**)
- S. Sun, **Z. Yan** and J. Zambreno, "Experiments in Attacking FPGA-Based Embedded Systems using Differential Power Analysis", *in Proceedings of IEEE International Conference on Electro/Information Technology*, pages 7-12, 2008.

Journal Papers

- **J. Z. Yan** and C. Chu, "DeFer: Deferred Decision Making Enabled Fixed-Outline Floorplanning Algorithm", to appear in *IEEE Transactions on Computer-Aided Design.*
- S. Sun, **Z. Yan** and J. Zambreno, "Demonstrable Differential Power Analysis Attacks on Real-World FPGA-Based Embedded Systems", *Integrated Computer-Aided Engineering*, vol.16, no. 2, pp. 119-130, April 2009.

AWARDS AND HONORS

Awards from **IEEE/ACM Design Automation Conference**, Anaheim, CA
- DAC Best Paper Award Nomination (*top 11 out of 639 submitted papers*), June 2008

Awards from **Iowa State University**, Ames, IA
- Graduate Research Innovation and Progress Award, April 2008

Awards from **Renesas Technology Corp.**, Tokyo, Japan
- Honor of Ultra-Excellent Student (*top 1 out of 340*), March 2005

Awards from **Huazhong University of Sci. and Tech.**, Wuhan, China
- Excellent Undergraduate Thesis Award (*top 10 out of 340*), June 2006
- 1st Place of TianYing Cup on Digital Circuits Design Competition, December 2004
- Honor of Excellent Student (*top 10 out of 340*), March 2004
- Honor of Excellent Student (*top 10 out of 340*), September 2003

SKILLS SET

- Programming languages: C, C++, Perl, Python, MPI
- Hardware description languages: Verilog HDL, VHDL
- EDA tools: Altera Quartus, Cadence Encounter, Cadence Virtuoso, Xilinx EDK, Protel, ModelSim
- Algorithm development environments: Matlab
- System knowledge: Linux, Unix, Windows 9X, XP, NT

REFERENCES

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