

Viswanathan Subramanian

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OBJECTIVE

An internship position that furthers my knowledge and experience in computer architecture, embedded system design and/or Analog and Digital VLSI design/testing/verification.

EDUCATION

Iowa State University

PhD (Beginning date: Fall 2005)

Department of Computer Engineering, GPA **4.0/4.0**

Birla Institute of Technology and Science, India

B.E.(Hons.) (Graduation date: Spring 2003)

Department of Electronics & Instrumentation Engineering, GPA 8.41/10.0

FULL-TIME EMPLOYMENT/ INTERNSHIP

ST Microelectronics, Noida, India**Aug03 – Jul05*****Associate Design Engineer, Full-time******Intellectual Property (IP) Design Team, DVD/STB Division, Home Entertainment Group***

- Design, implementation and verification of single cycle memory access in ST20-C1 microcontrollers.
- Implementation and verification of 2-way cache organization in place of direct mapped implementation in ST20-C2 microcontrollers.
- Front end design (Synthesis, timing analysis, equivalence checking, and verification) of various IPs. Worked on few DFT issues too.
- Conversion of bus protocol from I2C serial bus to ST's own STBus interface in Direct Digital Amplifier (DDX) IP.
- Worked on Video Decode Accelerator IP and made modification to the architecture to support changes in video formats.
- Provided support for ST20 family of microprocessors whenever issues occurred. Fixed few critical bugs.

ST Microelectronics, Noida, India**Jan03 – Jul03*****Associate Design Engineer, Intern***

- Performed an exhaustive study of the internal micro-architecture of the ST20-C1 32-bit RISC-based microprocessor.
- Modified the existing RTL to make it functionally equivalent to the structural schematic netlist of the same microprocessor.
- Verified the modified RTL, and performed equivalence checking using formal verification tools to prove functional equivalence.

RESEARCH EXPERIENCE

Fault Tolerant Microprocessor Architectures

- Implemented a novel fault masking methodology to protect microprocessor control logic. The implementation was done in OpenRISC 1200 from OpenCores.org.

Reliable Overclocking to Achieve High Performance in Superscalar Processors

- Researching on timing error detection and correction in overclocked superscalar processors
- Developed tool set for DLX processor – DLX GCC Compiler and DLX Assembler
- Compilation of SPEC CPU 2000 benchmarks for DLX scalar and superscalar processor
- Designed an algorithm that will increase the contamination delay of the datapath to allow reliable overclocking
- Researching on a clocking strategy that will allow switching between clocks without any penalty
- Building an external clock generation circuit that will aid dynamic frequency scaling

PUBLICATIONS

Conference Publications

- Ganesh T S, Viswanathan Subramanian and Arun Somani " SEU Mitigation Techniques for Microprocessor Control Logic", EDCC, 2006
- Viswanathan Subramanian, Mikel Bezdek, Prasad Avirneni and Arun Somani "Superscalar Processor Performance Enhancement Through Reliable Dynamic Clock Frequency Tuning", IEEE/IFIP DSN, 2007

SKILLS

- Programming Languages/HDLs: C, Verilog, VHDL, SpecC, SystemC
- Scripting Languages : Perl, Shell Scripting, Tool command language(tcl)
- Operating Systems: Windows, Linux, UNIX, Solaris
- CAD Tools:
 - Simulation: NcSim, Verilog XL, Modelsim, Quartus, Spectre(ADE)
 - Synthesis: Synopsys Design Compiler, Cadence BuildGates
 - Timing Analysis: Synopsys Primetime
 - Equivalence Checking: Synopsys Formality
 - Layout: Cadence Virtuoso Layout Editor, Tanner Tools
 - Place & Route: SOC Encounter
- FPGA: Xilinx Virtex II ISE and Platform Studio
- Others (minimal experience): Assembly language programming, C++, Verisity Specman Elite, PSpice, Matlab, Labview, Javascript, Oracle PL/SQL, VB, VB script

COURSE WORK

Graduate Course Work

- Computer Systems Architecture, Analog & Digital VLSI Design, Reconfigurable Computing Systems, Embedded Computer Systems, Fault Tolerant Systems, Advanced Topics in Computer Architecture, Design & Analysis of Algorithms, Physical Design of VLSI Systems, Analog VLSI Circuit Design, Synthesis and Optimization of Digital Circuits, Statistical Theory for Research Workers
- Course topper for Computer Systems Architecture, Reconfigurable Computing Systems, Embedded Computer Systems, Fault Tolerant Systems

TERM PROJECTS

- Design and implementation of efficient pattern matching algorithm for network intrusion detection system on FPGA. (Iowa State University, Ames, Iowa; Graduate Term project for Course Reconfigurable Computing Systems - Fall 2005)
- Design and implementation of a Transceiver. This design was fabricated using MOSIS AMI 0.6 micron process, and the chip was validated for correctness. (Iowa State University, Ames, Iowa; Graduate Term project for Course Integrated Circuit Design - Fall 2005)
- Design and implementation of a Counterflow Pipeline processor. (Iowa State University, Ames, Iowa; Graduate term project for course Advanced Computer Architecture – Spring 2006)
- Design and implementation of fault tolerant techniques such as triple modular redundancy to protect microprocessor datapath. (Iowa State University, Ames, Iowa; Graduate term project for course Fault Tolerant Systems – Spring 2006)
- Modeled an Anti-Lock Braking system using SpecC and SystemC. (Iowa State University, Ames, Iowa; Graduate term project for course Embedded System Design – Spring 2006)
- Design and implementation of Non-stochastic fixed-outline floorplanning tool. (Iowa State University, Ames, Iowa; Graduate term project for course Physical Design of VLSI Systems – Fall 2006)
- Implementation of a synthesis paradigm to minimize variance in path delays of digital logic circuits. (Iowa State University, Ames, Iowa; Graduate term project for course Synthesis & Optimization of Digital Circuits – Spring 2007)
- Implementation of Two Stage OpAmp and 12-bit Successive Approximation Register ADC. (Iowa State University, Ames, Iowa; Graduate term project for course Analog VLSI Circuit Design – Spring 2007)

HONORS AND ACHIEVEMENTS

- Received Student Travel Grant Award for IEEE/IFIP DSN 2007
- Invited member, Tau Beta Pi, Academic Honor Society, ISU
- President for Sankalp, a Campus Student Organization at ISU 2007-2007
- ST Site Level Trainer for Synopsys Formal Verification tool Formality
- Co-Editor of Instrumentation Forum's magazine IMAGE 2005 at BITS-Pilani
- Recipient of Merit Cum Need Scholarship in BITS, Pilani

References: available upon request