

Viswanathan Subramanian

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OBJECTIVE A position that exercises and enhances my knowledge and experience in computer architecture, embedded system design and/or analog and digital VLSI design.

EDUCATION *Doctor of Philosophy*, Computer Engineering
Iowa State University, Ames, IA, USA
Jerry R. Junkins Chair Fellow
Expected Graduation: December 2009, GPA 4.0/4.0
Thesis Title: Timing Speculation and Adaptive Reliable Overclocking Techniques for Aggressive Computer Systems
Major Professor: Dr. Arun Somani

Bachelor of Engineering (Hons.), Electronics & Instrumentation
Birla Institute of Technology and Science, Pilani, India
Graduation date: June 2003, GPA 8.41/10.0

EXPERIENCE *NVIDIA Corporation*, Santa Clara, CA, USA Summer 2008
Summer Intern

Display-FPGA

- Developed a synthesizable RTL verification environment for a frame buffer design targeted for FPGA.
- Developed the test plan, design, and implementation in two months.
- Built the environment conforming to Nvidia verification standards.
- Developed random tests for regression testing.

GT216-Timing

- Worked on timing closure of four partitions in GT216 graphics chip.

ST Microelectronics, Greater Noida, India August 2003 - July 2005
Associate Design Engineer, Full-time

Intellectual Property (IP) Design Team, Home Entertainment Group (DVD/STB)

- Implementation and verification of single cycle memory access in ST20-C1 microcontrollers.
- Verification of 2-way set associative cache organization in place of direct mapped implementation in ST20-C2 microcontrollers. Modified testbench and tests accordingly.
- Front end design (Synthesis, timing analysis, equivalence checking, and verification of netlist) of various IPs. Worked on few DFT issues too.
- Conversion of bus protocol from I2C serial bus to STs own STBus interface in Direct Digital Amplifier IP.
- Worked on Video Decode Accelerator IP and made modification to the architecture to support changes in video formats.
- Provided support for ST20 family of microprocessors whenever issues occurred. Fixed few critical bugs.

ST Microelectronics, Greater Noida, India

January 2003 - July 2003

Intern

IP Design Team, Consumers and Microcontrollers Group (DVD)

- Performed an exhaustive study of the internal micro-architecture of the ST20-C1 32-bit RISC-based microprocessor.
- Modified the existing RTL to make it functionally equivalent to the structural schematic netlist of the same microprocessor.
- Verified the modified RTL, and performed equivalence checking using formal verification tools to prove functional equivalence.

**RESEARCH
EXPERIENCE**

Dependable Computing and Networking Laboratory

Iowa State University, Ames, IA

Summer 2006 - Present

Research Assistant

Reliable Overclocking to Achieve High Performance in Superscalar Processors

- Worked on timing error detection and correction in overclocked superscalar processors
- Analyzed a hardware model of an alpha processor to estimate error rates at overclocked frequencies
- Modified SimpleScalar Toolset to analyze performance benefits achieved through reliable overclocking
- Developed a dynamic clock tuning methodology using phase locked loops available in Xilinx Virtex 5 FPGAs
- Developed tool set for DLX processor DLX GCC Compiler and DLX Assembler
- Analyzed the benefits of reliable overclocking in a 2-issue superscalar DLX processor implemented in FPGA
- Designing an algorithm that will increase the contamination delay of the datapath to allow reliable overclocking

Fault Tolerant Architectures

- Developed a novel approach based on organized pipeline redundancy to enhance both hardware reliability and performance. Conjoined pipeline architecture supports overclocking, provides concurrent error detection and recovery capability for soft errors, intermittent faults and timing errors, and flags permanent silicon defects.
- Developed Soft Error Mitigation (SEM) and Soft and Timing Error Mitigation (STEM) schemes for protecting combinational logic blocks from soft errors. Our first technique (SEM), based on distributed and temporal voting of three registers, unloads the soft error detection overhead from the critical path of the systems. Our second technique (STEM) adds timing error detection capability to guarantee reliable execution in aggressively clocked designs that enhance system performance by operating beyond worst-case clock frequency.
- Implemented a novel fault masking methodology to protect microprocessor control logic. The strategy for protecting static instruction dependent control signals utilizes a distributed cache of the history of the control bits along with the Triple Modular Redundancy (TMR) concept, while the opcode dependent control signals are protected by a distributed cache which is used to flag errors. Dynamic signals are protected by selective duplication of datapath components.

Thermal Aware Microprocessor Design

- Developing novel architecture based on DVFS and reliable overclocking to manage temperature and performance of microprocessors

**TEACHING
EXPERIENCE**

Teaching Assistant

Fall 2005 - Spring 2006

Electrical and Computer Engineering Department, Iowa State University, Ames, IA

- Laboratory assistant and homework evaluator for CprE 305: Computer Organization and Design course

PUBLICATIONS *Conference/Workshop Publications*

- Ganesh T S, **V. Subramanian** and A. K. Somani, “*SEU Mitigation Techniques for Microprocessor Control Logic*,” Sixth European Dependable Computing Conference, Coimbra, Portugal, Oct 2006
- **V. Subramanian**, M. Bezdek, N. D. Avirneni and A. K. Somani, “*Superscalar Processor Performance Enhancement Through Reliable Dynamic Clock Frequency Tuning*,” IEEE/IFIP Dependable Systems and Networks, Edinburgh, Scotland, Jun 2007
- **V. Subramanian**, N. D. Avirneni and A. K. Somani, “*Conjoined Processor: A Fault Tolerant High Performance Microprocessor*,” IEEE Workshop on Silicon Errors in Logic - System Effects, Austin, TX, Mar 2008
- **V. Subramanian** and A. K. Somani, “*Conjoined Pipeline: A Fault-Tolerant High Performance Microarchitecture*,” Pacific Rim International Symposium on Dependable Computing, Taipei, Taiwan, Dec 2008
- N. D. Avirneni, **V. Subramanian**, and A. K. Somani, “*Soft Error Mitigation Schemes for High Performance and Aggressive Designs*,” IEEE Workshop on Silicon Errors in Logic - System Effects, Stanford, CA, Mar 2009
- P. Ramesh, **V. Subramanian**, and A. K. Somani, “*Thermal Management in Reliably Overclocked Systems*,” Poster Paper, IEEE Workshop on Silicon Errors in Logic - System Effects, Stanford, CA, Mar 2009
- **V. Subramanian**, P. K. Ramesh and A. K. Somani, “*Managing the Impact of On-chip Temperature on the Lifetime Reliability of Reliably Overclocked Systems*,” The Second International Conference on Dependability (DEPEND 2009), Athens, Greece, Jun 2009
- N. D. Avirneni, **V. Subramanian**, and A. K. Somani, “*Low Overhead Soft Error Mitigation Techniques for High-Performance and Aggressive Systems*,” IEEE/IFIP Dependable Systems and Networks, Lisbon, Portugal, Jul 2007

Publications - Under Review and In Progress

- **V. Subramanian**, P. K. Ramesh and A. K. Somani, “*Speculation-based Reliable Overclocking: A Cost-efficient Competitive Alternative to Technology Scaling*,” MICRO-42 (Under Review)
- P. K. Ramesh, **V. Subramanian** and A. K. Somani, “*Beyond traditional DVFS - A system level study for thermal control, energy efficiency and performance augmentation*,” ICCD 2009 (Under Review)
- **V. Subramanian**, P. K. Ramesh and A. K. Somani, “*Characterizing Timing Specualtion Based Adaptive Reliable Overclocking Techniques*,” (Work in Progress)
- **V. Subramanian** and A. K. Somani, “*Fault Tolerant Aggressive Systems*,” (Work in Progress)
- **V. Subramanian** and A. K. Somani, “*Exploiting Short Paths for Performance Acceleration in Reliably Overclocked Systems*,” (Work in Progress)

**COMPUTER
SKILLS**

Programming Languages/HDLs: C, Verilog, VHDL, SpecC, SystemC

Scripting Languages: Perl, Tcl, Shell Scripting

Operating Systems: Windows, Linux, Solaris, UNIX

CAD Tools:

- Simulation: NcSim, Verilog XL, Modelsim, Quartus, Spectre

- Synthesis: Synopsys Design Compiler, Cadence BuildGates
- Timing Analysis: Synopsys Primetime
- Equivalence Checking: Synopsys Formality
- Layout: Cadence Virtuoso Layout Editor, Tanner Tools
- Place & Route: SOC Encounter

FPGA: Xilinx Virtex-II, Virtex-5 ISE and Platform Studio, Altera Stratix

Others (minimal experience): Assembly language programming, C++, Verity Specman Elite, PSpice, Matlab, Labview, Javascript, Oracle PL/SQL, VB, VB script

GRADUATE COURSE WORK

Computer Systems Architecture, Analog & Digital VLSI Design, Reconfigurable Computing Systems, Embedded Computer Systems, Fault Tolerant Systems, Advanced Topics in Computer Architecture, Design & Analysis of Algorithms, Physical Design of VLSI Systems, Analog VLSI Circuit Design, Synthesis and Optimization of Digital Circuits, Statistical Theory for Research Workers, Design and Analysis of Experiments

Course topper for Computer Systems Architecture, Reconfigurable Computing Systems, Embedded System Design, Fault Tolerant Systems

CASE STUDIES

- Design and implementation of efficient pattern matching algorithm for network intrusion detection system on FPGA. (Iowa State University, Ames, Iowa; Graduate Term project for Course Reconfigurable Computing Systems - Fall 2005)
- Design and implementation of a Transceiver. This design was fabricated using MOSIS AMI 0.6 micron process, and the chip was validated for correctness. (Iowa State University, Ames, Iowa; Graduate Term project for Course Integrated Circuit Design - Fall 2005)
- Design and implementation of a Counterflow Pipeline processor. (Iowa State University, Ames, Iowa; Graduate term project for course Advanced Computer Architecture Spring 2006)
- Design and implementation of fault tolerant techniques such as triple modular redundancy to protect microprocessor datapath. (Iowa State University, Ames, Iowa; Graduate term project for course Fault Tolerant Systems Spring 2006)
- Modeled an Anti-Lock Braking system using SpecC and SystemC. (Iowa State University, Ames, Iowa; Graduate term project for course Embedded System Design Spring 2006)
- Design and implementation of Non-stochastic fixed-outline floorplanning tool. (Iowa State University, Ames, Iowa; Graduate term project for course Physical Design of VLSI Systems Fall 2006)
- Implementation of a synthesis paradigm to minimize variance in path delays of digital logic circuits. (Iowa State University, Ames, Iowa; Graduate term project for course Synthesis & Optimization of Digital Circuits Spring 2007)
- Implementation of Two Stage OpAmp and 12-bit Successive Approximation Register ADC. (Iowa State University, Ames, Iowa; Graduate term project for course Analog VLSI Circuit Design Spring 2007)

**HONORS
AND
ACHIEVE-
MENTS**

ECPE Graduate Research Innovation and Progress Award, ISU 2007
Invited member, Tau Beta Pi, Academic Engineering Honor Society, ISU
President of Sankalp, a Campus Student Organization at ISU 2007-2008
Treasurer of Sankalp, a Campus Student Organization at ISU 2006-2007
ST Site Level Trainer for Synopsys Formal Verification tool Formality
Treasurer of Instrumentation Forum, a Student Organization at BITS-Pilani 2001-
2002
Co-Editor of Instrumentation Forums magazine IMAGE 2005 at BITS-Pilani
Recipient of Merit Cum Need Scholarship in BITS, Pilani