

NATARAJAN VISWANATHAN

3625 Duval Rd, Apt 725
Austin, TX - 78759
(515) 451-1250 (C)

email: nataraj@iastate.edu
web: <http://www.public.iastate.edu/~nataraj>

RESEARCH INTERESTS

VLSI Physical Design

- Algorithms and methodologies for floorplanning, placement and timing optimization.
- Development of a simultaneous placement and timing optimization framework.

EDUCATION

Ph.D.	Computer Engineering	Iowa State University, Ames, IA	Expected 2008
M.S.	Computer Engineering	Iowa State University, Ames, IA	2003
	Thesis: An Efficient Analytical Placement Algorithm Using Cell Shifting, Iterative Local Refinement and a Hybrid Net Model.		
B.E.	Electronics and Communication	Karnataka Regional Engg. College, India	2001

EXPERIENCE

RESEARCH

Technical Co-op IBM Austin Research Lab. Feb 2006 - Present

- Member of the research team working on the IBM Placement Driven Synthesis (PDS) tool.
- Developed an efficient wirelength and congestion driven Force-Directed placement/floorplanning algorithm to be used within PDS.
- Currently working on a timing-driven placement flow within the PDS framework.

Graduate Research Assistant Iowa State University Aug 2004 - Present

- Extended the FastPlace standard-cell placement algorithm to handle mixed-size placement, and address placement blockage and placement congestion constraints.
- Developed an efficient and robust legalization algorithm for macro-block as well as standard-cell legalization.
- Implemented a multi-level global placement framework to improve the scalability and solution quality of FastPlace and handle multi-million gate designs.
- Current research is on developing fast buffer insertion and gate sizing techniques and to incorporate them within a placement framework. The goal is to yield an integrated placement and timing optimization framework to handle timing-driven placement.

Graduate Research Assistant Iowa State University Aug 2002 - Oct 2003

- Proposed a Hybrid Net Model, a Cell Shifting technique and an Iterative Local Refinement technique to be used within an analytical placement framework.
- Based on the above techniques, developed FastPlace, an efficient, wirelength driven, analytical placement algorithm for large scale standard-cell circuits.

Undergraduate Research Project Karnataka Regional Engg. College Aug 2000 - May 2001

- Developed and implemented a heuristic algorithm to determine the variable ordering required to minimize the number of nodes in a BDD and generate a Reduced Order Binary Decision Diagram (ROBDD).

INDUSTRY

CAD Engineer - Process Micron Technology, Inc. Oct 2003 - Jul 2004

- Supported the Physical Verification tool deck used for CMOS Image Sensor Design. The work involved coding for the Hercules tool.
- Developed the framework to create and transfer Project Design Kits for Imaging designs spanning multiple process generations. Work involved coding in Perl and using the Synchronicity tool.

- Performed the layout and verification of individual CMOS Image Sensor pixels and full chip verification for a fully functional next generation process test chip.
- Part of a team tasked with increasing the packing density of the digital logic present on Image Sensor chips. Work involved tuning EDA tools, and interacting with the process development, layout design and ASIC design teams to develop a new standard-cell library to double the existing packing density.

Intern Engineer - R&D CAD Micron Technology, Inc. May 2002 - Aug 2002

- Developed a new simulation flow for emerging technology. Work involved changing the existing netlist flow, simulation netlist manager and writing supporting programs for the new flow. It involved working with StarRC-XT and coding in Perl and Skill.
- Extracted parasitic information related to standard-cells and a fully routed cell in the Standard Parasitic Exchange Format (SPEF). This was used for cell characterization and to estimate interconnect delays in Verilog Simulations.

PUBLICATIONS AND PATENTS

Book Chapters

N. Viswanathan, M. Pan and C. Chu, "FastPlace: An Efficient Multilevel Force-Directed Placement Algorithm," *Modern Circuit Placement: Best Practices and Results*, Springer, G.-J. Nam and J. Cong (editors).

Journals

N. Viswanathan and C. C.-N. Chu, "FastPlace: Efficient Analytical Placement using Cell Shifting, Iterative Local Refinement and a Hybrid Net Model," *IEEE Transactions Computer-Aided Design*, vol. 24, no. 5, pages 722-733, 2005.

Conferences

N. Viswanathan, G.-J. Nam, C. J. Alpert, P. Villarrubia, H. Ren and C. Chu, "RQL: Global Placement via Relaxed Quadratic Spreading and Linearization," In *Proc. Design Automation Conference*, pages 453-458, 2007. **(Nominated for DAC Best Paper Award)**

N. Viswanathan, M. Pan and C. Chu, "FastPlace 3.0: A Fast Multilevel Quadratic Placement Algorithm with Placement Congestion Control," In *Proc. Asia and South Pacific Design Automation Conference*, pages 135-140, 2007.

N. Viswanathan, M. Pan and C. Chu, "FastPlace 2.0: An Efficient Analytical Placer for Mixed-Mode Designs," In *Proc. Asia and South Pacific Design Automation Conference*, pages 195-200, 2006.

M. Pan, N. Viswanathan and C. Chu, "An Efficient and Effective Detailed Placement Algorithm," In *Proc. IEEE/ACM International Conference on Computer-Aided Design*, pages 48-55, 2005.

N. Viswanathan, M. Pan and C. Chu, "An Efficient Analytical Placement Algorithm for Mixed-Mode Designs in the Presence of Placement Blockages," In *Proc. SRC TECHCON 2005*, Oct. 2005.

N. Viswanathan and C. C.-N. Chu, "FastPlace: Efficient Analytical Placement using Cell Shifting, Iterative Local Refinement and a Hybrid Net Model," In *Proc. International Symposium on Physical Design*, pages 26-33, 2004. **(ISPD 2004 Best Paper Award)**

Patents

C. C.-N. Chu and N. Viswanathan, "FastPlace Method for Integrated Circuit Design", Submitted.

C. J. Alpert, G.-J. Nam, H. Ren, P. G. Villarrubia and N. Viswanathan, "Method to Reduce the Wirelength of Analytical Placement Techniques by Modulation of Spreading Force Vectors", Submitted.

AWARDS AND HONORS

IBM Early Tenure Inventor Award, 2007.

ECpE Graduate Excellence Fellowship, Department of Electrical and Computer Engineering, Iowa State University, 2004.

Premium for Academic Excellence Award (PACE), Iowa State University, 2004 - 2005.

Best Paper Award, International Symposium on Physical Design, 2004.

72nd in a Nation-wide Science Talent Search Examination, conducted when in 12th grade.

SKILL SET

Programming: C, Unix Shell, Perl, Skill, SpecC, Verilog, Assembly.

EDA Tools: Cadence Tool Kit, SOC Encounter, Synopsys Tool Kit, Hercules, Star-RCXT, Hspice, Silicon Ensemble.

Operating Systems: Linux, Unix, Windows 9X, XP, NT.

REFERENCES

Dr. Chris C.-N. Chu
Associate Professor
Electrical and Computer Engineering
Iowa State University
Ames, IA - 50011
(515) 294-3490
cnchu@iastate.edu

Dr. Charles J. Alpert
Technical Lead, Design Tools
IBM Austin Research Lab.
Austin, TX - 78758
(512) 838-1045
alpert@us.ibm.com