

Vipul Katyal

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Dept. of Electrical and Computer Engineering
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Objective

Full time employment in the area of Analog and Mixed VLSI.

Summary

Electrical engineer with solid research background in Analog and Mixed Signal (AMS) VLSI and numerical methods in Electromagnetics. Strong programming skills in Fortran, C++ and Matlab. Education in fabrication processes and VLSI. Performed roles of team lead and team member on various projects. Effective problem solver with demonstrated verbal and written communication skills. Recipient of all but dissertation award (ABD) and academic excellence award (PACE award). Member of IEEE Solid State Society and Phi Kappa Phi Honor Society. All India Rank in JEE (Joint Entrance Examination) of 367 out of 150000 (0.245 percentile) for the admission process of Indian Institute of Technologies (IITs), India. 13th/14th Electrical Engineering B.S. class rank at IIT-Kanpur out of graduating class of 70 students.

Education

Ph.D., Electrical Engineering, Iowa State University, Spring 2008	GPA 3.72/4.0
M.S., Electrical Engineering, Iowa State University, Fall 2002	GPA 3.90/4.0
B.S., Electrical Engineering, with minor in Computer Science, I.I.T. Kanpur, May 2000	GPA 8.70/10

Work Experience

Co-op at National Semiconductor Corporation from May 2006 – Dec. 2006. Responsibilities included architectural and design implementation of PWM Temperature Sensor, design of input-output digital pins with built in threshold levels, reference current source and chip testing of Digital Temperature Sensor.

Research assistant under Dr. R. L. Geiger and Dr. D. J. Chen from Jan. 2003 onwards (Iowa State University). Worked on pipelined A/D design specifically on the MDAC design (amplifier and comparator designs and optimizations) looking at KT/C noise constraints and its over-range requirements. Apart from pipelined A/D design, worked on successive A/D design, low power supply voltage design strategies of an amplifier using charge-pumps, linear ramp generation for a Built in Self test and threshold control of Schmitt triggers (Input receivers). Also worked on chip testing and debugging the problems associated with the successive A/D design project.

Research assistant under Dr. J. R. Bowler from Jan. 2001 till Dec. 2002 (Iowa State University). Worked on edge element techniques and finite element methods for the discretization of the flaw region for better performance of the sensor array response. Also worked on race track eddy current probe formulation by fast Fourier transform and magnetic shell model for flaw and crack detection inside a metal surface for the development of instruments for Aviation industry.

Research assistant under Dr. P. K. Chatterjee from Aug 1999 till April 2000 (IIT-Kanpur, India). Worked on design and implementation of an amplifier (pre and post) using Schematic and circuit board for analog optical communication Link of 200 MHz.

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Ph.D. Thesis

Low power high gain high speed amplifier design methodologies and offset minimization techniques of dynamic comparators for a Pipeline ADC application along with hysteresis controllable Schmitt trigger.

Technical Skills

- Verilog-A/MS, Verilog, VHDL, C/C++, Matlab, Maple, Fortran, Pascal, MS Access, Visual Basic
- AMS Designer, Cadence tools, Synopsys tools, Silicon Ensemble tools, Spice, Spectre, SystemView, Espresso (digital logic minimizer), Mathematica and WinEdt
- Linux, Unix (HPUX) and Windows XP

Interests

- Data converters including pipelined A/Ds and its building blocks including low offset dynamic comparators, amplifier optimization, over-range protection schemes, KT/C constraint design challenges.
- CMOS Schmitt triggers design strategies.
- References (voltage and current).
- Temperature Sensors.
- Amplifiers including low voltage supply under threshold and positive feedbacks.
- Built in Self Test (BIST).

Publications

- Vipul Katyal, Randall L. Geiger and Degang J. Chen, “Adjustable Hysteresis CMOS Schmitt Triggers,” Paper submitted for International Symposium on Circuits and Systems, Seattle, USA, 2008.
- Vipul Katyal, Randall L. Geiger and Degang J. Chen, “A New High Precision Low Offset Dynamic Comparator for High Resolution High Speed ADCs,” Asia Pacific Conference on Circuits and Systems, Singapore, 2006.
- Vipul Katyal, Randall L. Geiger and Degang J. Chen, “A New Low Offset Dynamic Comparator for High Resolution High Speed ADC Application,” Semiconductor Research Corporation’s Student Symposium 2006.
- Vipul Katyal, Yu Lin, Randall L. Geiger and Degang J. Chen, “Power Dependence of Feedback Amplifier on Op-Amp Architecture,” TECHCON, Portland, Oregon, 2005.
- Vipul Katyal, Yu Lin, Randall L. Geiger and Degang J. Chen, “Statistical Modeling of Over-Range Protection Requirement for a Switched Capacitor Inter-Stage Gain Amplifier,” Midwest Symposium on Circuits and Systems, Cincinnati, Ohio, 2005.
- Yu Lin, Vipul Katyal, Randall L. Geiger and Degang J. Chen, “New Over-Range Protection Scheme in Pipelined Data Converters,” Midwest Symposium on Circuits and Systems, Cincinnati, Ohio, 2005.
- Vipul Katyal, Yu Lin and Randall L. Geiger, “Power Dependence of Feedback Amplifier on Op-Amp Architecture,” International Symposium on Circuits and Systems, Kobe, Japan, 2005.
- Yu Lin, Vipul Katyal and Randall L. Geiger, “KT/C Constrained Optimization of Power in Pipeline ADCs,” International Symposium on Circuits and Systems, Kobe, Japan, 2005.

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Publications

- Vipul Katyal and John R. Bowler, "Magnetic Sensor Array for Eddy Current Field Measurement with a Racetrack Coil Excitation," Electromagnetic Nondestructive Evaluation (VIII) IOS Press, Amsterdam 2004.
- John R. Bowler, Vipul Katyal, Guliemo Rubinacci, Antonello Tamburrino, Thomas C.-P. Chiu and Marcus Johnson, "Simulation and Design of Eddy-Current Array Sensors for NDE of Hidden Corrosion," Conference on Aging Aircraft, San Francisco, California, 2002. (Presentation only)
- Vipul Katyal and John R. Bowler, "Simulation of Eddy Current Detection of Corrosion Using Sensor Array," Quantitative Non-Destructive Evaluation Conference, Bellingham, Washington, 2002.
- John R. Bowler Norio Nakagawa, Thomas C.-P. Chiu and Vipul Katyal, "Simulation of Eddy Current Interaction with Hidden Corrosion," Quantitative Non-Destructive Evaluation Conference, Brunswick, Maine, 2001.

Relevant Course Projects

- "5.3 GHz BFSK Direct Conversion Receiver Design," VLSI Communication Circuits.
- "Direct Conversion Receiver Design for 802.11b Application," VLSI Communication Circuits.
- "Filter Design for an adaptive equalizer technique for 75 ohms coaxial cable," Filter Design and Applications.
- "Calibration techniques for thermometer coded current-mode D/A," Data Converter Circuits.
- "Design of high bandwidth fully differential positive feedback amplifier," Analog VLSI Design.
- "Design and layout implementation of programmable waveform generator," Introduction to Integrated Circuit Design.
- "Fabrication of PMOSs and BJTs on Silicon wafers," Introduction of Microelectronic Fabrication.
- "Matlab simulation on Dispersive Materials using Frequency-Dependent Finite-Difference Time-Domain Formulation," Topics in Electromagnetics.
- "Matlab simulation on 2-D Shielded Micro-strip Analysis using Finite Element Method," Topics in Electromagnetics.
- "Matlab simulation and presentation on Equivalent Surface Current Density on a Square Cylinder in presence of TM – Wave," Topics in Electromagnetics
- "Matlab simulation and presentation on TE Modes in a Circular Cross Section Wave Guide," Advanced Electromagnetic Field Theory I.
- "Designed and Implemented Hotel Database using MS Access and Visual Basic," Principles of Database Systems.

Teaching Experience

Worked as teaching assistant for Electromagnetic Applications in Computer Systems in the department of Electrical Engineering, ISU (Fall 2000 and Spring 2001).

References

Available on request.